Polaris Total Radio™, A highly Integrated RF Solution for GSM/GPRS and EDGE

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Abstract – **This paper describes how the constant goal to achieve higher functionality at lower cost drives innovation in chip set architectures and accomplishments in integration in RF semiconductors. This paper will discuss a complete GSM/GPRS radio system that has been implemented by use of highly integrated circuits that exhibit levels of integration and features unparallel in the industry. A new, proven radio architecture and it's performance will be shown including the integration of VCOs and associated loop filters, system oscillator, power management, power amplifier power control circuitry, auxiliary DACs and more.**
System details will be show how the elimination of IF filters is supported by the use of either zero IF (ZIF) or very low IF (VLIF) radio architectures. A comparison between ZIF and VLIF is presented. The use of a fractional N synthesizer based digital GMSK modulator and DSP based digital channel filters will be discussed. Additionally, the benefits derived by use of digital radio-to-baseband interfaces are discussed and the implications to the industry are presented.

I. Introduction

With the introduction of General Packet Radio Services (GPRS), near term roll out of Enhanced Data Rates for GSM Evolution (EDGE), and the technical challenges of UMTS and other third generation cellular system, semiconductor companies are scrambling to provide cost-effective chipsets that meet the broad range of requirements for these complex communications standards.

In support of the above market opportunities, RF Micro Devices has developed the Polaris Total Radio™, a GSM/GPRS chipset employing several innovations that will bring direct benefit to handset designers and the industry. See figure 1. Additionally, Polaris will form the basis for Polaris II, an RF chipset for GSM/GPRS and EDGE. By providing consistency across chipsets, handset developers will be able to implement products covering a broad range of standards while minimizing changes in software and hardware.

This article discusses many of the design innovations implemented in the Polaris chipset and how some of these innovations set a new standard in integration and component count.

II. Chipset Description

The Polaris chipset was developed to provide both very low IF (VLIF) and direct conversion radio (DCR) architectures. VLIF systems are less sensitive than direct conversion systems to DC offsets and even order distortion products since any resulting DC components generated by the mixer does not fall in the desired pass-band. Typically the low IF frequency is chosen to be one half the channel spacing to be offset from any DC components and to avoid large alternate channel interferers. It should be noted that VLIF is very well suited to cellular standards, including GSM/GPRS, where the system specified limits control the adjacent channel interference.

Direct conversion can be beneficial when the optimum channel bandwidth exceeds approximately 85kHz half channel bandwidth, typically required for 8-PSK reception

III. RF2716 Receive Front End

Within the RF2710/RF2716, four LNAs are provided, each internally matched to 100 ohms differential. Supported frequency bands include the US cellular, EGSM, DCS and US PCS bands. Handset manufacturers can produce dual, triple or quad-band handsets using a single chipset populating only the appropriate functions. The fully integrated VCO requires no external support components and works in conjunction with the RF6001's integrated loop filter and programmable frequency synthesizer. The internal VCO runs at the 4GHz frequencies and is divided by two to provide the high-band frequencies and divided by four to provide low-band frequencies.

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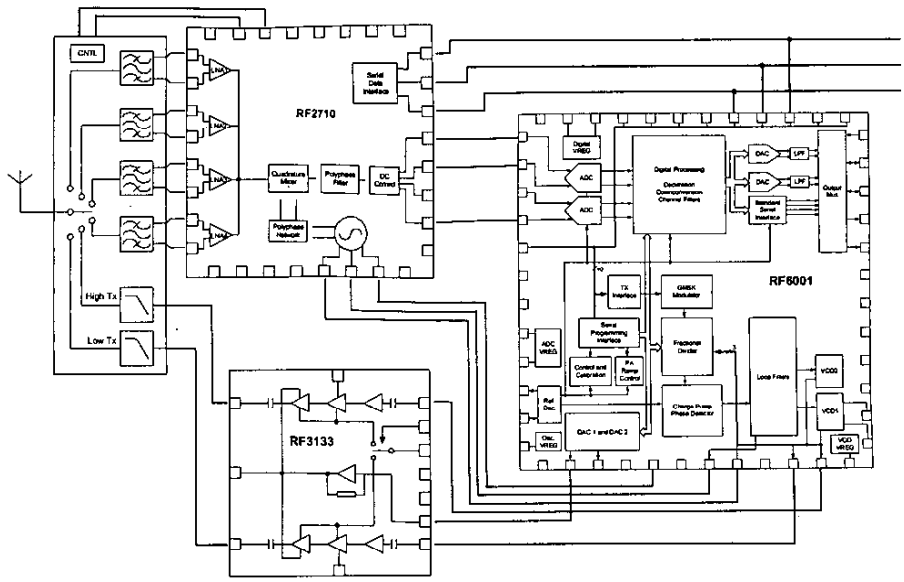

Fig. 1. Polaris Total Radio™ Block Diagram

When in VLIF mode, the quadrature mixers down convert the signals to 100kHz IF and pass them through a three-stage polyphase filter. This filter helps reject interfering signals and protects the dynamic range of the A/D converters in the RF6001. Each of the three polyphase-filter stages provides gain and is controlled as defined in the gain control registers set via the serial data interface.

A coarse DC offset correction scheme has been included in the RF2716 to reduce offsets caused by various sources including device mismatches and LO feed through. The DC offset levels are brought to below 20mV in the RF2716 and are further reduced to approximately 2 milli-volts in the RF6001.

Four general purpose I/Os have been provided in the RF2716 to allow control of various switchplexer Tx/Rx and band select control pins. The general-purpose I/Os' logic states are defined via the serial-data interface registers. Availability of these I/O pins reduces the number of signal lines crossing from the baseband into the radio.

IV. WIDE DYNAMIC RANGE RECEIVER

The chipset's receive path includes dual wide dynamic range (12.9 bit ENOB) A/D converters at the inputs to the RF6001. The wide dynamic range A/Ds provide several benefits to the system, and when combined with use of the digital interface, can reduce the frequency of automatic gain control (AGC) writes from the baseband, simplifying operation and the amount of associated software.

For baseband devices that can accommodate signals from a few milli-volts up to approximately one volt, nominal gain is held from reference sensitivity of –109dBm to –57dBm before the gain is modified. The additional headroom in the A/D converters supports fast up and down fades with specific ability to accommodate large down fades. This ultimately can improve the handset's ability to hold a call under slow moving mobile applications.

The polyphase filter stages within the RF2716 provide 70dB of analog gain control range. An additional 14dB gain step is provided at the LNAs. A digital gain control register provides for an additional 90dB of gain control, in 6dB increments. This allows the user the ability to keep the digital or analog output voltage at a constant level to accommodate baseband devices that have limited receive dynamic range. All gain control is performed via a three-wire serial data interface.

V. DIGITAL FILTERING

Due to the varying amount of filtering offered by industry baseband devices, all filter functions are provided within the chipset to remove dependencies on any specific baseband device.

In order to provide filtering for large off-channel signals and to protect the A/D converters from being overdriven, initial filtering is done with analog polyphase filters within the RF2716 immediately following down conversion from RF. Once in the digital domain, the signal is further processed including down conversion to DC, anti aliasing, anti droop and digital channel filtering.

Benefits achieved by use of digital channel filters include no group delay variance, stable performance over voltage, temperature and process tolerances, less silicon area and lower power consumption when compared to analog filters. Digital filters also provide the ability to dynamically modify the channel bandwidth of the system to accommodate different modes of operation or to select a specific bandwidth to accommodate a specific baseband. The RF6001 includes eight selectable bandwidths from 80 to 135kHz half channel bandwidths. See figure 2.0

Once in the digital domain, it was easy to provide digital outputs that could be used by the baseband instead of using historic analog I/Q signals. However, to enable compatibility with the largest number of existing baseband devices, both digital and analog I/Q interfaces are provided.

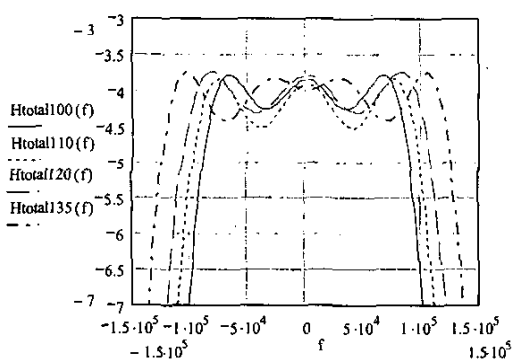

Fig. 2 Channel Filters 100 – 135kHz

VI. RF6001 TRANSMIT SECTION

The RF6001 transmit section includes both analog I/Q and digital baseband interfaces, a fractional N synthesizer, a digital GMSK modulator, dual power VCOs plus a power amplifier ramp control DAC.

VII. FRACTIONAL N SYNTHESIZER

The fractional N synthesizer, within the RF6001, provides the core for the receive and transmit phased locked loops (PLLs). The synthesizer provides programmable R (reference frequency) and N (VCO) dividers. The N divider contains a dual modulus prescaler and digitally spur-compensated fractional sequence generator to allow fine frequency steps. Frequency steps of 1.55Hz can be achieved enabling the digital GMSK modulator described below.

In support of the fast start up and channel hop times required for GPRS and EDGE, a deadzone-free phase detector is incorporated to provide fast, low-jitter locking performance. The ability to hop frequencies and settle to within 100Hz of the final frequency can be achieved in just 140 microseconds. A lock detect output pin is provided to validate proper PLL performance.

The RF6001 includes integrated loop filters for both the high- and low-band output VCOs in the transmit section and the receive VCO in the RF2716. The loop filters can be set to automatically calibrate to account for processing and environmental variations.

VIII. FRACTIONAL N BASED DIGITAL MODULATOR

In the transmit path, the Polaris chipset uses a digital modulator. At the center of the modulator is the fractional N synthesizer, tracing frequency versus time, to provide the appropriate signal to the integrated output VCOs. This modulator significantly simplifies the transmit section eliminating the need for the translational loop circuitry seen in the majority of GSM/GPRS chipset solutions. The primary benefits of the digital modulator are low power consumption. The complete transmit chain, including VCOs, but excluding the PAM, uses 45mA compared to 70 to 90mA for translational loop systems and higher for direct launch RF modulators. The low power consumption is largely achieved by use of digital circuits and the elimination of circuit blocks including the I/Q modulator, mixer, phase detector, and IF synthesizer and associated VCO.

The integrated power VCOs provides an output noise of better than –162dBc/Hz @ 20MHz offset, eliminating the need for all filters before or after the power amplifier. This performance allows direct connection from the VCO outputs to the power amplifier inputs.

When using the transmit digital interface, digital Non-Return-to-Zero (NRZ) data can be taken directly from the baseband eliminating the need for the baseband's modulator, gaussian filter, and A/D converters found in many of today's baseband devices. Alternatively, the

RF6001 has been designed to accept GMSK modulated analog I/Q signals from the baseband.

IX. PA RAMP CONTROL DAC

The RF6001 includes a 14-bit power amplifier ramp control D/A converter. This function has been designed to take advantage of a very efficient indirect closed-loop power-control scheme implemented in many of RFMD's power amplifier modules. The power ramp waveform is defined based on sixteen bit settings in programmable registers within the RF6001. The ramp down waveform is symmetrical to the ramp up waveform. A conceptual timing diagram of the PA ramp control system is illustrated in Figure 3.0

Polaris supports GPRS operation by providing the capability to change power levels in sequential time slots. This enables the subsequent time slot level to be set during the present slot enabling differing output power levels from slot to slot. Integrating the PA ramp DAC function into the RF6001 further reduces the control lines required between the baseband and the radio and reduces demands on the baseband processor.

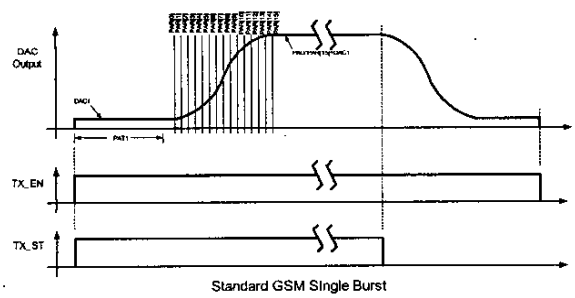

Fig. 3.0 PA RAMP DAC

XI. DIGITAL OR ANALOG INTERFACES

The Polaris chipset offers digital and analog I/Q interfaces to the baseband in both receive and transmit paths. Analog interfaces are included in the chipset to support use with the broadest number of baseband devices. The digital interface provides three specific selectable modes of operation accommodating various baseband devices. The use of digital filtering in the receive path, and the use of the digital GMSK modulator in the transmit path naturally support digital interfaces between the baseband and the RF sections.

One benefit of using digital interfaces is the ability to eliminate the A/D and D/A converters commonly found in baseband devices. This approach could allow the development of pure digital baseband products. The baseband could then be migrated to the next-generation process-technology, eliminating the need to redesign any associated analog functions.

XII. RF3133 POWER AMPLIFIER MODULE

The RF3133 is a quad-band power amplifier module designed using GaAs HBT process technology. It uses an indirect, closed-loop power-control scheme, which is designed to regulate the collector voltages of the amplifier stages. The collector voltages of the amplifiers are regulated to a multiplied Vramp signal. The amplifier stages provide constant bias and stay in saturation across all power levels. This results in two primary benefits: maximizing power added efficiency (PAE) at maximum power levels and eliminating output power variations due to sensitivity to battery voltage levels.

No external components are required for biasing, matching or power control, assisting in the overall goal to minimize the component count of the radio. The ramp DAC within the RF6001 directly drives the Vramp pin on the PA module, providing over 35dB of output power control range. Maximum output power is +35dBm for the EGSM band and +33dBm for the DCS and PCS bands. Band Select and Transmit Enable pins can also be driven directly for the RF6001, minimizing signals between the baseband and radio functions.

XIV. CONCLUSION

As seen above the Polaris chipset offers several advantages over many of today's existing GSM/GPRS chipset solutions. The use of the most appropriate technology provides for the best performance in system sensitivity, power consumption and PAE while achieving the minimum cost. Availability of digital RF to Baseband interfaces introduces the opportunity to change the system partitioning using pure digital baseband solutions. The very low number of components required to create a complete radio transceiver enables handset suppliers to lower system costs while significantly reducing time to market and associated development costs.